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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,387	12/08/2003	Mahibur Rahman	SC12882ZC	2615

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EXAMINER	
FLORES, LEON	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,387	RAHMAN ET AL.	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/08/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) *16-19 & 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

Claim 21 is objected to because of the following informalities: In claim 21, the limitation "sequence generator having an input coupled to the second input of the first

summation" does not concord with figure 1. Figure 1 depicts a PN sequence generator having **an output, not its input**, coupled to the second input of summation 44.

Therefore, the limitation should be rewritten as "sequence generator having an output coupled to the second input of the first summation". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 26, it is not clear to the examiner what the applicant is trying to contemplate with the following limitation: ***"an analog input signal over a predetermined frequency range approximately at the analog filter's center frequency to a magnitude of the analog input signal over a predetermined frequency range approximately at the bandwidth frequency of the analog filter".*** Is the applicant trying to say that there are two different predetermined frequencies or just one.

For the purpose of art consideration on the merits, this limitation will be construed as comparing the magnitude of two analog signals each at a predetermined frequency.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims (1-4, 9-12, 14-15, 20-24 & 26) are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsurumi et al (hereinafter Tsurumi) (US Patent 6,639,909 B1), and in view of Webster (US Patent 6,304,615 B1).

Re claim 1, Tsurumi discloses a method for controlling a bandwidth of an analog filter circuit (See fig. 61: elements 415 & 416 & see col. 39, lines 34-64) comprising: performing a DC offset correction operation in the analog filter circuit to generate a DC offset correction signal (See fig. 61: element 20 & 21); holding the DC offset correction

signal in the analog filter circuit (See fig. 61: elements 43 & 44); adding a training signal to the DC offset correction signal (See fig. 61: element 414); and determining a magnitude of a filtered input signal using the training signal and the DC offset correction signal (See fig. 62); and determining a magnitude of the filtered input signal at a predetermined frequency using the training signal and the DC offset correction signal(See fig. 62); comparing the difference to a predetermined threshold value to generate an error metric (See Fig. 62: elements 415(416). In this configuration, a signal is compared with a reference signal to generate an error signal.); and using the error metric to adjust the bandwidth frequency of the analog filter circuit. (See Fig. 61: elements 415 & 416 & see col. 39, lines 34-64)

But the reference of Tsurumi fails to specifically disclose determining a difference between the magnitudes of the filtered input signal and the filtered input signal at the predetermined frequency, and comparing the difference to a predetermined threshold.

However, Webster does. (See Fig. 8: 110) Webster discloses an automatic gain control system. The system is comprised of a DC restorer, which restores the DC component of the input pulse train, an equalizer, two filters, two level detectors, which detects the amplitude of both filters, and a difference element, which takes the difference between the amplitude of both filters and outputs, as a result, an error signal.

Taking the combined teachings of Tsurumi & Webster as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated the step of taking the difference of the two magnitude into the system of Tsurumi, for the benefit of

yielding an error signal which ultimately controls the automatic gain controller and the equalizer.

Re claim 2, the combination of Tsurumi & Webster further discloses that wherein determining a magnitude of a filtered input signal further comprises: low pass filtering the filtered input signal to generate a low pass filtered signal; and determining a magnitude of the low pass filtered signal. (In Tsurumi, see Fig. 61: the output of elements 22 & 23. Furthermore, the input signal has already been filtered by element 15, and filtered again by the low pass filters 22 & 23.)

Re claim 3, the combination of Tsurumi & Webster further discloses that wherein determining a magnitude of a filtered input signal at the predetermined frequency further comprises: mixing the filtered input signal with a sinusoidal signal at the predetermined frequency to produce a baseband signal (In Tsurumi, see Fig. 61: element 18); low pass filtering the baseband signal around the predetermined frequency to produce a low pass filtered input signal located at the predetermined frequency (In Tsurumi, see Fig. 61: elements 22 & 23); and determining a magnitude of the low pass filtered input signal at the predetermined frequency. (In Tsurumi, see fig. 61: the output of elements 22 & 23.)

Re claim 4, the combination of Tsurumi & Webster further discloses that wherein the predetermined frequency is a bandwidth frequency equal to about the -3 dB (decibel) comer of the analog filter. (In Tsurumi, see col. 39, lines 34-51)

Re claim 9, the combination of Tsurumi & Webster further discloses wherein the training value is generated using a pseudo-random sequence generator. (In Tsurumi, see fig. 61: 414. Tsurumi teaches that a test signal generator generates a test signal which is added to the DC offset to correct the DC offset associated with the incoming signal. Furthermore, One skilled in the art would know that one way to generate training signals is by using a PN generator.)

Re claim 10, the combination of Tsurumi & Webster further discloses wherein the analog filter circuit is an active resistor-capacitor (RC) filter. (In Tsurumi, see col. 39, lines 48-51. Furthermore, one skilled in the art would know that filters are comprised of either active/passive resistors-capacitors. These components are responsible for the adjustment of the poles and zeros in a filter.)

Re claim 11, the combination of Tsurumi & Webster further discloses wherein the analog filter circuit is a gm-C type filter. (In Tsurumi, see col. 39, lines 40-51. Furthermore, one skilled in the art would know that one way to adjust the cut-off frequency of an analog filter is by controlling its gain GM.)

Re claim 12, the combination of Tsurumi & Webster further discloses wherein the method is performed in a spread spectrum code-division multiple access (CDMA) receiver. (In Tsurumi, see col. 10, lines 9-13. Furthermore, if the training signal or test

signals are generated using a PN generator, then we can say that the receiver constitutes a CDMA system.)

Re claim 14, the motivation for combining the references of Tsurumi & Webster has already been established in claim 1, therefore, the combination of Tsurumi & Webster further discloses a filter circuit comprising: an analog filter element having an input for receiving an analog input signal (In Tsurumi, see fig. 61: the input of 22 & 23), an output for providing a filtered output signal (In Tsurumi, see fig. 61: the output of 22 & 23), and a control input for receiving a control signal for adjusting a bandwidth frequency of the analog filter element to a predetermined bandwidth frequency (In Tsurumi, see figure 61: the output of element 415 is inputted to element 22 & 23); an analog-to-digital converter having an input coupled to the output of the analog filter element, and an output (In Tsurumi, see figure 61: 3); a digital tracking loop having an input coupled to the output of the analog-to-digital converter, and an output coupled to the control input of the analog filter element (In Tsurumi, see fig. 61: element 40 is coupled to the output of an A/D converter and has a output connected to element 22 & 23), the digital tracking loop for comparing a magnitude difference to a predetermined threshold to generate an error signal (the combined teachings of Tsurumi & Webster teaches this limitation), the error signal used to generate the control signal (In Tsurumi, see fig. 61: the output of element 415), where the magnitude difference is determined by subtracting a first magnitude of the analog input signal over a predetermined

frequency range to a second magnitude of the analog input signal over the predetermined frequency range. (In Webster, see fig. 8)

Claim 15 has been analyzed and rejected in view of claim 10.

Re claim 20, the combination of Tsurumi & Webster further discloses a DC offset correction circuit having an input coupled to the output of the analog-to-digital converter, and an output (In Tsurumi, see Fig. 61: elements 41 & 43 as a whole constitute a DC offset correction unit, and its input is connected to the output of element 3.); a first summation circuit having a first input coupled to the output of the DC offset correction circuit, a second input, and an output (In Tsurumi, see fig. 61: element 410 or 411 is connected to the output of elements 43 and 44, and it has a second input and an output.); a digital-to-analog converter having an input coupled to the output of the summation circuit, and an output (In Tsurumi, see fig. 61: element 5 is connected to the output of element 410 and 411.); and a second summation circuit having a first input coupled to the output of the digital-to-analog converter (In Tsurumi, see fig. 61: element 20 & 21 are connected to the output of element 5.), a second input for receiving an analog signal, and an output coupled to the input of the analog filter element. (In Tsurumi, see fig. 61: element 20 & 21 are connected to the output of two mixers, and are connected to the input of elements 22 & 23.)

Re claim 21, the combination of Tsurumi & Webster further discloses a random number sequence generator having an input coupled to the second input of the first summation circuit. (In Tsurumi, see fig. 61: 414)

Claim 22 has been analyzed and rejected in view of claim 9.

Re claim 23,the combination of Tsurumi & Webster further discloses single or multiple sinusoidal tones generator having an input coupled to the second input of the first summation circuit. (In Tsurumi, see fig. 61: 16 & 17)

Claim 24 has been analyzed and rejected in view of claim 12.

Claim 26 has been analyzed and rejected in view of claim 14. Furthermore, the frequencies of the incoming signals can be adjusted at any desired frequency by means of a mixer located at the receiver.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsurumi et al (hereinafter Tsurumi) (US Patent 6,639,909 B1) and Webster (US Patent 6,304,615 B1), as applied to claim 1 above, and further in view of Li et al. (hereinafter Li)(US Publication 2003/0007574 A1)

Re claim 5, the combination of Tsurumi & Webster fails to disclose filtering the error signal using a loop filter having a predetermined bandwidth.

However, Li does. (See fig. 4) Li discloses a coefficient updating circuit that is comprised of two squares, and adder, a low pass filter, and a memory to store the updated coefficient. After obtaining the error signal from the result of an adder, the error signal is filtered by a low pass filter.

Taking the combined teachings of Tsurumi, Webster & Li as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated a filter into the system of Tsurumi, as modified by Webster, in the manner as claimed, for the benefit of eliminating any noise associated with comparator unit.

7. **Claims (6-8) are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsurumi et al (hereinafter Tsurumi) (US Patent 6,639,909 B1) and Webster (US Patent 6,304,615 B1), as applied to claim 1 above, and further in view of Becker et al. (hereinafter Becker)(US Patent 5,612,975)**

Re claim 6, the combination of Tsurumi & Webster fails to disclose that wherein the error metric is used to select filter coefficients from a look-up table, the filter coefficients being used to adjust the bandwidth of the analog filter circuit. However, Becker does. (See fig. 9: elements 253 & 270 & col. 11, lines 1-25, & col. 8, lines 39-64)

Becker discloses a system capable of adjusting the bandwidth of a pair of low pass filters. The system includes a coefficient memory unit for storing coefficients, and a processor for adjusting the bandwidth of the low pass filters.

Taking the combined teachings of Tsurumi, Webster & Becker as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated a storing device into the system of Tsurumi, as modified by Webster, in the manner as claimed, for the benefit of adjusting the bandwidth of the filters.

Re claim 7, the combination of Tsurumi, Webster & Becker further discloses that wherein the error metric is used to select filter coefficients from a look-up table, the filter coefficients being used to adjust pole and zero locations of the analog filter circuit. (In Tsurumi, see col. 39, lines 34-64. One skilled in the art would know that in order to adjust the bandwidth of a filter one must adjust the values of the resistors and capacitors in the filter.)

Re claim 8, the combination of Tsurumi, Webster & Becker further discloses that wherein the error metric is used to select filter coefficients from a look-up table, the filter coefficients being provided to the analog filter circuit on a multi-bit bus. (In Tsurumi, see fig. 61: elements 415 & 416. Furthermore, one skilled in the art would know that this operation must be performed very rapidly in order to avoid adjacent channel interference.)

8. **Claims (13 & 25) are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsurumi et al (hereinafter Tsurumi) (US Patent 6,639,909 B1) and Webster (US Patent 6,304,615 B1), as applied to claim 1 above, and further in view of Holenstein et al. (hereinafter Holenstein) (US Publication 2003/0199264 A1)**

Re claim 13, the combination of Tsurumi & Webster fails to disclose that wherein the method is performed in a spread spectrum code-division multiple access (CDMA) transmitter. However, the Holenstein does. (See paragraph 50.) Holenstein discloses a system for canceling DC offset for mobile station modems having direct conversion architectures. This system, can also be a transceiver, is capable of detecting and correcting DC offset in a signal.

Taking the combined teachings of Tsurumi, Webster, & Holenstein as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated a transmitter into the system of Tsurumi, as modified by Webster, for the benefit of reducing manufacturing costs and providing an optimized system capable of receiving and transmitting signals without DC offsets.

Claim 25 has been analyzed and rejected in view of claim 13 above.

Allowable Subject Matter

9. Claims 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In claim 16, the further limitation of "wherein the digital tracking loop further comprises: a first low pass filter having an input coupled to the output of the analog-to-digital converter, and an output; a first magnitude determination unit having an input coupled to the output of the low pass filter, and an output for providing the first magnitude of the analog input signal; a mixer circuit having an input coupled to the output of the analog- to-digital converter, and an output; a second low pass filter having an input coupled to the output of the mixer circuit, and an output; a second magnitude determination unit having an input coupled to the output of the second low pass filter, and an output for providing the second magnitude of the analog input signal over the predetermined frequency range located approximately at the predetermined bandwidth frequency; a summation element having an input for receiving the first and second magnitudes, and an output for providing the magnitude difference; and a comparator having a first input for receiving the magnitude difference, a second input for receiving the predetermined threshold, and an output for providing the error signal".

Claims 17-19 depend on 16.

Contact

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
January 24, 2007

David Payne
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